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# A Numerical Technique for Removing Residual Gate-source Capacitances When Extracting Parasitic Inductance for GaN High Electron Mobility Transistors (HEMTs)

**by Benjamin Huebschman and Pankaj B. Shah**

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The design of monolithic microwave integrated circuits (MMIC) is dependent on the ability to generate accurate device models. Prior knowledge of the external parasitic components is required to determine the small signal model of the intrinsic device. A simple technique for determining and correcting for the gate-source capacitance during the extraction of the series inductance will be presented. This technique has worked well when integrated into existing small signal extraction procedures.


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AlGaN, extraction, GaN, gate inductance, high electron mobility transistor (HEMT), intrinsic device, parasitic, small-signal model

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## 1. Introduction

As gallium nitride (GaN) high electron mobility transistors (HEMTs) begin to realize their performance potential, and to transition from experimental devices to commercial applications, accurate device models are required to design monolithic microwave integrated circuits (MMICs) based on this technology (*1–3*). There have been a number of reports of successful methods for generating small signal models (*4, 5*). The technique, which will be outlined further, follows a recently published method, but modifies the step during which the series parasitic elements are calculated.

To determine the series parasitics, the gate is forward-biased with respect to the drain and the source, and $V_{ds}$ is set to zero. According to existing parasitic extraction methods, when a device is biased in this manner, the intrinsic device can be approximated as a short circuit. However, in (*4*) it is observed that a residual gate source capacitance remains that appears to be in series with the gate elements. An earlier method proposes that the effect from the capacitor is small and can be ignored, while (*5*) calculates a predicted value for the capacitance under this bias. Ignoring $C_{gs}$, or calculating the value based on knowledge of the device fabrication, produces frequency dependent values for the equivalent circuit model components that do not correspond with the proper frequency response of lumped elements. In this report, we describe a numerical technique that has proven useful for directly determining $C_{gs}$ from measured data in order to determine series parasitics.

## 2. Theory

The parasitic shunt (pad) capacitances were determined according to the procedure described in (*4*). The device is forward-biased and the S-parameters were measured. The shunt capacitances were de-embedded and the data are transformed into a z-matrix. The simplified model neglecting channel resistance of the device in the forward-bias condition is shown in figure 1.

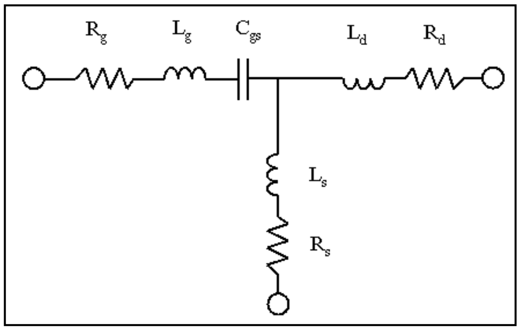


Figure 1. Simplified equivalent circuit model for HEMT in the forward bias with pad capacitances removed.

The Z parameters for the circuit in figure 1 are given by

$$z_{11} = R_g + R_s + j\omega(L_g + L_s) - \frac{j}{\omega C_{gs}} \tag{1}$$

$$z_{12} = z_{21} = R_s + j\omega L_s \tag{2}$$

$$z_{22} = R_d + R_s + j\omega(L_d + L_s)\,.$$

Based on these equations, the parameter values can be calculated:

$$R_s = \mathrm{Re}(z_{12}) \tag{3}$$

$$R_g = \mathrm{Re}(z_{11}) - R_s \tag{4}$$

$$R_d = \mathrm{Re}(z_{22}) - R_s \tag{5}$$

$$L_s = \frac{\mathrm{Im}(z_{22})}{\omega} \tag{6}$$

$$L_d = \frac{\mathrm{Im}(z_{22})}{\omega} - L_s \tag{7}$$

$$L_g = \frac{\mathrm{Im}(z_{11})}{\omega} - L_s + \frac{1}{\omega^2 C_{gs}}\,. \tag{8}$$

These values are directly calculated from the measured data, with the exception of the last equation. $C_{gs}$ is an unknown value. With the knowledge of $C_{gs}$, the entire set of series parasitic elements can be determined.

The technique for determining $C_{gs}$ is as follows:

$$X_{11} = \mathrm{Im}(z_{11}) \tag{9}$$

$$\frac{X_{11}}{\omega} = (L_s + L_g) - \frac{1}{C_{gs}\omega^2} \tag{10}$$

$$\frac{d\frac{X_{11}}{\omega}}{d\omega} = \frac{2}{C_{gs}\omega^3} \tag{11}$$

$$C_{gs} = \frac{2}{\omega^3 \frac{d\frac{X_{11}}{\omega}}{d\omega}} = \frac{2}{\omega^3 \frac{\Delta\frac{\mathrm{Im}(z_{11})}{\omega}}{\Delta\omega}} \tag{12}$$

The numerical differentiation of $\mathrm{Im}(z_{11})/\omega$ was performed using the following equation:

$$\frac{\Delta x_i}{\Delta\omega} = \frac{x_{i+1} - x_{i-1}}{2\Delta\omega} \tag{13}$$

It should be mentioned that the differentiation of discrete values is the equivalent of a high-pass filter. If the data are noisy, the derivative might be dominated by the high frequency components of the noise. The easiest way to eliminate this problem is to reduce the number of samples, which functions as a filter for the noise.

## 3. Measured Results and Analysis

The modified extraction process was performed on several devices from several different wafers. A comparison of the values of Lg as determined by different methods is shown in figure 2. The calculations differ by the manner in which $C_{gs}$ is calculated. The method described in (*5*) disregards the value of $C_{gs}$. In (*4*), $C_{gs}$ is calculated based on the knowledge of the fabrication process of the device. The numerically determined value follows the procedure described above.

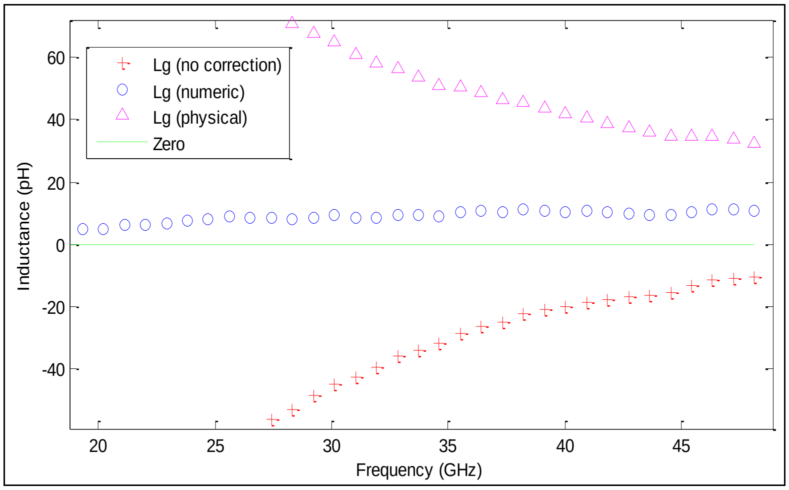


Figure 2. Comparison of calculated gate inductance as determined by different methods.

The series parasitic values are plotted as a function of frequency in figure 3. As is shown in figures 2 and 3, the value Lg, when calculated using this technique, does not show a frequency dependence, which is consistent with a linear equivalent circuit model.

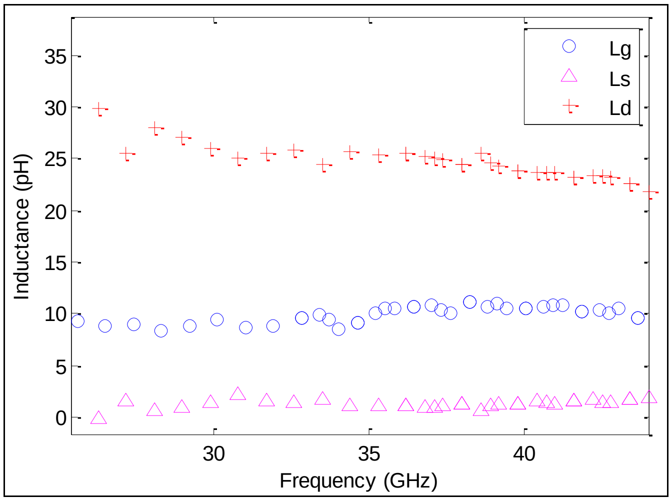


Figure 3. Extracted parasitic inductances plotted versus frequency.

The extracted values were used in the model shown previously to reproduce the S-parameters. The parasitic shunt capacitances were embedded. The modeled S-parameters are compared to the measured S-parameters of the forward-biased device and close agreement is observed, as shown in figure 4.

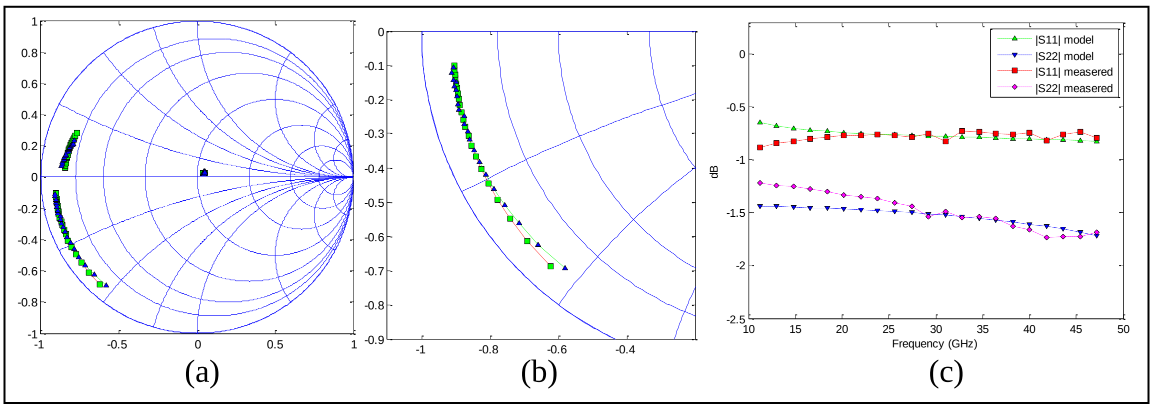


Figure 4. Modeled S-parameters compared with measured values (a) measured and modeled S-parameters plotted on the Smith chart, (b) measure and modeled S11 plotted on the Smith chart, and (c) magnitude (dB) for S11 and S22 from 10 to 50 GHz.

The new technique has a number of advantages:

1. The calculated value of Lg does not show the frequency dependence that is observed when Lg is determined by the other methods. This is more consistent with the linear model of the inductor when used in the equivalent circuit model.

2. This method determines the gate inductance based on the frequency response of the z-parameter and does not require any special information about the device or additional measurement to determine $C_{gs.}$
3. The lack of frequency dependence in the calculated value of Lg results in a measurement that can be performed at lower frequencies without the requirement for a Q band vector network analyzer (VNA). This reduces the capital requirements to perform the measurement.
4. This method can be applied generally to any series resistor, inductor, and capacitor circuit. The example provided demonstrates the usefulness when extracting parasitics from GaN HEMTs, but the method described could be applied to any unknown series RLC circuit.

## 4. Conclusion

A method of determining the residual capacitance as a necessary step to calculating the series parasitic elements was examined. A new method for determining the residual gate capacitance based on the frequency dependence of the impedance is being used at ARL. The value for $C_{gs}$ was used to calculate a series gate inductance that does not depend on frequency. The results of the model reproduced from the equivalent circuit model agree well with the measured data. The method described can be applied generally to determine the component values for a RLC, for which the impedance parameters are known or can be determined.

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